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PATENT & TRADEMARK OFFICE

Attorney's Docket No.: 14069-014001

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	: Arnd Kilian et al.	Art Unit	: 2832
Serial No.	: 10/699,981	Examiner	: Tuyen Nguyen
Filed	: November 3, 2003	Conf. No.	: 5328
Title	: THREE-DIMENSIONAL INDUCTIVE MICRO COMPONENTS		

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

BRIEF ON APPEAL

(1) Real Party in Interest

The real party in interest is Hymite A/S.

(2) Related Appeals and Interferences

None.

(3) Status of Claims

Claims 14-16, 21-23 and 33-34 stand rejected.

Claims 1-13, 17-20 and 24-32 were withdrawn from consideration as the result of a restriction requirement. Applicant requests that, in the event claim 16 is allowed, dependent claims 17-20 be allowed as well. Similarly, in the event claim 21 is allowed, dependent claims 24-26 should also be allowed.

Applicant appeals the rejections of claims 14-16, 21-23 and 33-34.

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(4) Status of Amendments

All proposed amendments have been entered. No amendments have been filed subsequent to the final Office action.

(5) Summary of Claimed Subject Matter

Independent claim 14 recites a method comprising forming a plurality of conductive lines each of which extends along a bottom surface of a trench in a substrate, along opposite sidewalls of the trench, and along an upper surface of the substrate on both sides of the trench.

An example is illustrated in FIG. 3 of the pending application which shows a trench 34 in a substrate 32. Conductive lines 38 are formed on a bottom surface 36 and extend along opposite sidewalls of the trench. Portions 40 of each conductive line 38 extend along an upper surface of the substrate 32. *See* Specification, page 5, line 19 – page 6,line 8.

The method of claim 14 also recite using a wire bonding technique to provide conductive interconnections among portions of the conductive lines to form a plurality of windings for an inductive component wherein the windings are composed of the conductive lines and the conductive interconnections.

In the example of FIG. 3, conductive interconnections are identified by reference numeral 46. The conductive interconnections 36 connect portions 40 of the conductive lines 38 to form windings for an inductive components. *See* Specification, page 6, lines 10-16.

In the context of the pending application, a person of ordinary skill would understand that "wire bonding" is a technique that involves forming an interconnection with a wire. *See* B. Streetman, *Solid State Electronic Devices*, pp. 368-371 (Prentice-Hall 1980, 2nd ed.) (Exhibit 1). Particular examples of wire bonding include die bonding, thermocompression bonding and ultrasonic bonding. *Id.* Those same examples are expressly mentioned in the pending specification at page 6, lines 10-12. "Wire bonding" techniques do not include all techniques that provide metal or other conductive interconnections.

Independent claim 21 recites an electronic microcircuit comprising a substrate, a plurality of conductive lines, and "wire bonds" that interconnect portions of the conductive lines to define a plurality of windings for an inductive component. Each of the conductive lines extends along a bottom surface of a trench in the substrate, along opposing sidewalls of the trench, and along an upper surface of the substrate at both sides of the trench. An example is illustrated in FIG. 3. *See* also Specification, page 5, line 19 – page 6, line 16. A person of ordinary skill in the art would understand that "wire bonds" are formed by a wire bonding technique.

Applicant also points out that the office action apparently misinterpreted the following feature recited in claim 21: "wire bonds interconnecting portions of the conductive lines to define a plurality of windings . . ." Based on the remarks at the middle of page 2, the Office action appears to have understood that language as if the phrase "wire bonds interconnecting portions" refers to certain portions called "wire bonds interconnecting" portions. That is clearly incorrect in view of the claim language itself and the rest of the specification. Instead, the cited claim language refers to wire bonds that interconnect portions of the conductive lines. An example of that is illustrated in FIG. 3 of the pending application which show wire bonds 46 that interconnect portions 40 of the conductive lines 38.

The dependent claims define additional features of the invention.

(6) Grounds of Rejection

Claims 14-16, 21-23 and 33-34 stand rejected as anticipated under 35 U.S.C. § 102 by U.S. Patent No. 6,445,271 (Johnson).

(7) Argument

Anticipation under 35 U.S.C. § 102 requires that each and every limitation of the claimed subject matter be disclosed in a single reference. (*See* MPEP § 706.02(a)(IV), stating that "for anticipation under 35 U.S.C. 102, the reference must teach every aspect of the claimed invention either explicitly or inherently.")

During patent examination, the interpretation of the pending claims must be consistent with the interpretation that persons of ordinary skill in the art would reach in the context of the patent specification. (See MPEP § 2111-2111.01.)

In the present case, contrary to the Office action, and as discussed in greater detail below, the Johnson patent does not disclose using a "wire bonding technique" as recited in claim 14 and does not disclose "wire bonds" as recited in claim 21.

The Johnson patent discloses a three-dimensional micro-coil 12. Each includes metal 17 in a trench 19 of a lower substrate 11 and metal 16 on an upper wafer substrate 13 (*see* FIG. 1B). According to the Johnson patent, the substrates 11, 13 are bonded together by soldering 14, 15 (FIG. 1B; col. 5, lines 12-13).

The Office action's allegation that the metal 16 in the Johnson patent is formed by a "wire bonding technique" and corresponds to the claimed "wire bonds" indicates a failure to appreciate (1) that "wire bonding" and "wire bonds" are phrases that have well-defined meanings in the art, (2) that those meanings are consistent with the way those phrases are used in the pending application, and (3) that the interpretation of "wire bonding" and "wire bonds" as implied by the Office action is contrary to the ordinary meaning as a person of ordinary skill in the art would understand those phrases.

Furthermore, as discussed below, the interpretation implied by the Office action also is contrary to the use of the phrase "wire-bond" as used in the Johnson patent itself.

As explained above, in the context of the pending application, a person of ordinary skill would understand that "wire bonding" is a technique that involves forming an interconnection with a thin wire. *See* Specification, page 6, lines 10-12; FIG. 3; B. Streetman, *Solid State Electronic Devices*, pp. 368-371 (Prentice-Hall 1980, 2nd ed.) (Exhibit 1). Although the pending claims are not limited to the particular details of "wire bonding" disclosed in the Streetman text, it is clear that a person of ordinary skill in the art would understand that the Johnson patent does

not disclose "wire bonding" and "wire bonds" in connection with formation of the inductor coil(s) 12.

Instead, the Johnson patent (US 6,445,271) forms the inductor coil(s) by soldering together a substrate 11 and a wafer 13, each of which has a conductive pattern (16, 17) on its surface corresponding to portions of the inductor coil(s). The patterned layer 16 of metal on the upper wafer 13 (FIG. 1B) does not include wire bonds, and wire bonding is not used to form the inductor coil(s) in the Johnson patent.

The Johnson patent does, in fact, use the phrase "wire-bond," but not in connection with formation of the inductor itself. As stated in the Johnson patent, "For connections to external circuitry . . ., inductor 12 . . . can be connected to wire-bond pads 22" (*see* col. 5, lines 48). In other words, although the inductor 12 itself is not formed using wire bonds, pads 22 can serve as contacts for external connection using wire bonds, which allow the inductor to be coupled to external circuitry. That use of the phrase "wire-bond" is consistent with the way that phrase ordinarily is used in the field and, furthermore, is consistent with the way it is used in the pending claims. Furthermore, that use of the phrase "wire-bond" in the Johnson patent itself makes it clear that "wire bonds" and "wire bonding" are not used to form the inductor coil(s) in the Johnson patent. In particular, wire binding techniques are not used for the metal 16.

At least for the foregoing reasons, the pending claims are not anticipated by the Johnson patent.

Conclusion

It is believed that all of the pending claims have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper.

The brief fee of $250 is enclosed. Please apply any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: 7/17/06

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Appendix of Claims

14. A method comprising:

forming a plurality of conductive lines each of which extends along a bottom surface of a trench in a substrate, along opposite sidewalls of the trench, and along an upper surface of the substrate on both sides of the trench; and

using a wire bonding technique to provide conductive interconnections among portions of the conductive lines to form a plurality of windings for an inductive component wherein the windings are composed of the conductive lines and the conductive interconnections.

15. The method of claim 14 wherein providing conductive interconnections includes, for pairs of adjacent conductive lines, coupling a wire bond from a portion of a first metal line to a portion of a second metal line, wherein the portion of the first metal line is located along the upper surface of the substrate at a first side of the trench and the portion of the second metal line is located along the upper surface of the substrate at a second, opposite side of the trench.

16. The method of claim 15 including positioning a magnetic material in the trench as a core for the inductive component.

21. An electronic microcircuit comprising:

a substrate;

a plurality of conductive lines each of which extends along a bottom surface of a trench in the substrate, along opposing sidewalls of the trench, and along an upper surface of the substrate at both sides of the trench; and

wire bonds interconnecting portions of the conductive lines to define a plurality of windings for an inductive component wherein the windings are composed of the conductive lines and the wire bond interconnections.

22. The electronic microcircuit of claim 21 wherein each wire bond interconnects a portion of a first conductive line to a portion of a second conductive line, wherein the portion of

the first conductive line is located along the upper surface of the substrate at a first side of the trench and the portion of the second conductive line is located along the upper surface of the substrate at a second, opposite side of the trench.

23. The electronic microcircuit of claim 22 including a magnetic material in the trench as a core for the inductive component.

33. The method of claim 14 wherein the wire bonding technique includes using thermo compression.

34. The method of claim 14 wherein the wire bonding technique includes using ultrasound.

Evidence Appendix

Exhibit 1 is a copy of B. Streetman, *Solid State Electronic Devices*, pp. 368-371 (Prentice-Hall 1980, 2nd ed.). A copy of this exhibit was submitted previously with Applicant's Amendment in response to the action of May 17, 2005. A Declaration, including Exhibit 1 as an attachment, is submitted herewith.

Related Proceedings Appendix

None.

9.6.2 Wire Bonding

The earliest method used for making contacts from the monolithic chip to the package was the bonding of fine Au wires. Later techniques expanded wire bonding to include Al wires and several types of bonding processes. Here we shall outline only a few of the most important aspects of wire bonding.

If the chip is to be wire bonded, it is first mounted solidly on a metal lead frame (Fig. 9-33) or on a metallized region of an insulating substrate.

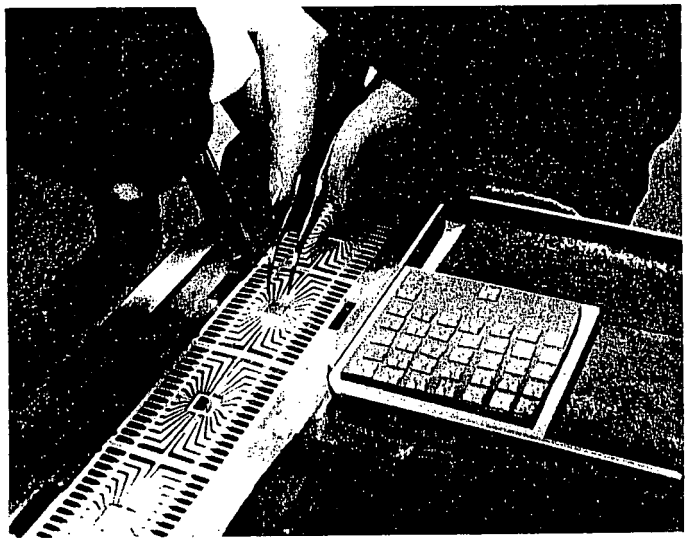

Figure 9-33. Mounting of chips in metal lead frames, in preparation for die bonding and contacting steps. (Photograph courtesy of Texas Instruments, Inc.)

In this process a thin layer of Au (perhaps combined with Ge or other elements to improve the metallurgy of the bond) is placed between the bottom of the chip and the substrate; heat and a slight scrubbing motion are applied, forming an alloyed bond which holds the chip firmly to the substrate. This process is called *die bonding* ("die," the singular form of "dice," is used interchangeably with "chip" to refer to the individual monolithic device). Once the chip is mounted, the interconnecting wires are attached from the various contact pads to posts on the lead frame (Fig. 9-34).

In Au wire bonding, a spool of fine Au wire (about 0.0007–0.002 inch diameter) is mounted in a *lead bonder* apparatus, and the wire is fed through a glass or tungsten carbide *capillary* (Fig. 9-35a). A hydrogen gas flame jet is swept past the wire to form a ball on the end. In *thermocompression*

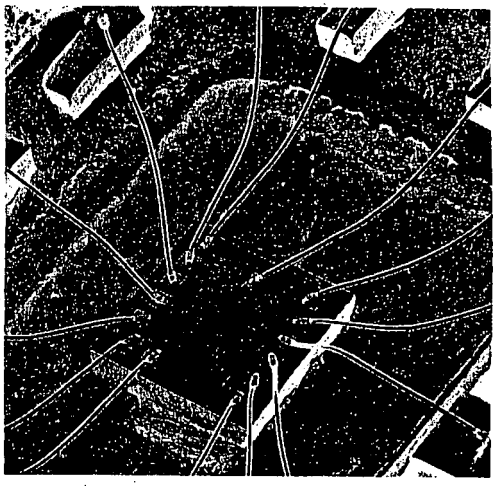

Figure 9-34. Attachment of leads from the Al pads on the periphery of the chip to posts on the lead frame. (Photograph courtesy of the National Bureau of Standards.)

bonding the chip (or in some cases the capillary) is heated to about 360°C, and the capillary is brought down over the contact pad. When pressure is exerted by the capillary on the ball, a bond is formed between the Au ball and the Al pad (Fig. 9-35b). Then the capillary is raised and moved to a post on the lead frame. The capillary is brought down again, and the combination of force and temperature bonds the wire to the post. After raising the capillary again, the hydrogen flame is swept past, forming a new ball (Fig. 9-35c); then the process is repeated for the other pads on the chip.

There are many variations in this basic method. For example, the substrate heating can be eliminated by *ultrasonic bonding*. In this method a tungsten carbide capillary is held by a tool connected to an ultrasonic transducer. When it is in contact with a pad or a post, the wire is vibrated under pressure to form a bond. Other variations include techniques for automatically removing the "tail" which is left on the post in Fig. 9-35c. When the bond to the chip is made by exerting pressure on a ball at the end of the Au wire, it is called a *ball bond* or a *nail-head bond*, because of the shape of the deformed ball after the bond is made.

Aluminum wire can be used in ultrasonic bonding; it has several advantages over Au, including the absence of possible metallurgical problems in bonds between Au and Al pads. When Al wire is used, the flame-off step is replaced by cutting or breaking the wire at appropriate points in the process. In forming a bond, the wire is bent under the edge of a wedge-shaped bonding tool (Fig. 9-35d). The tool then applies pressure and ultrasonic vibration, forming the bond (Fig. 9-35e and f). The resulting flat bond, formed

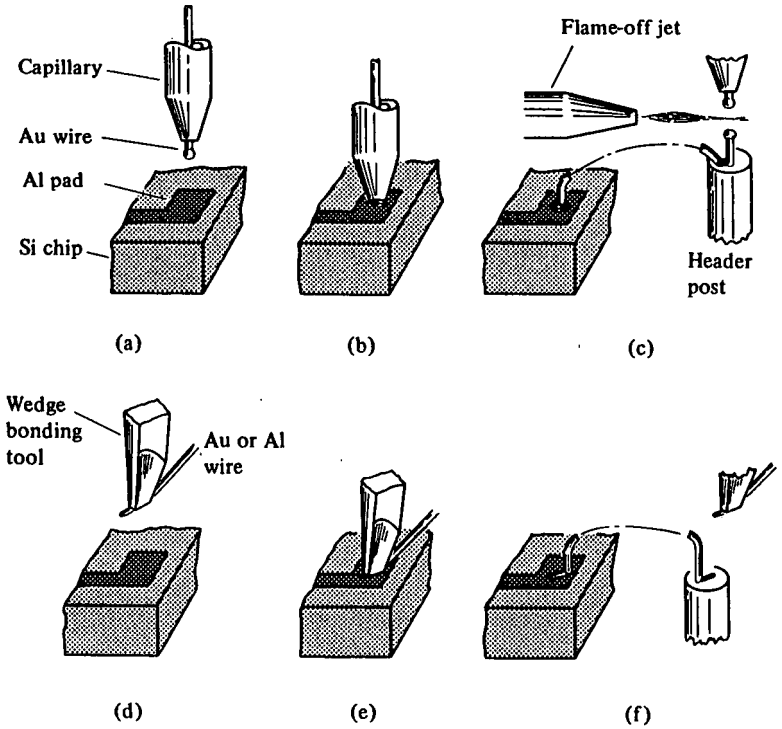

Figure 9-35. Wire bonding techniques: (a) capillary positioned over one of the contact pads for a ball (nail-head) bond; (b) pressure exerted to bond the wire to the pad; (c) post bond and flame-off; (d) wedge bonding tool; (e) pressure and ultrasonic energy applied; (f) post bond completed and wire broken or cut for next bond.

by the bent wire wedged between the tool and the bonding surface, is called a *wedge bond.* A closeup view of ball and wedge bonds is given in Fig. 9-36.

9.6.3 *Flip-Chip and Beam-Lead Techniques*

The time consumed in bonding wires individually to each pad on the chip can be overcome by several methods of simultaneous bonding. The *flip-chip* and the *beam-lead* approaches are typical of these methods. In each case, relatively thick metal is deposited on the contact pads before the devices are separated from the wafer. After separation, the deposited metal is used to contact a matching metallized pattern on the package substrate.

In the flip-chip method, "bumps" of solder or special metal alloys are deposited on each contact pad. These metal bumps rise about 50 μm above the surface of the monolithic chip. After separation from the wafer, each

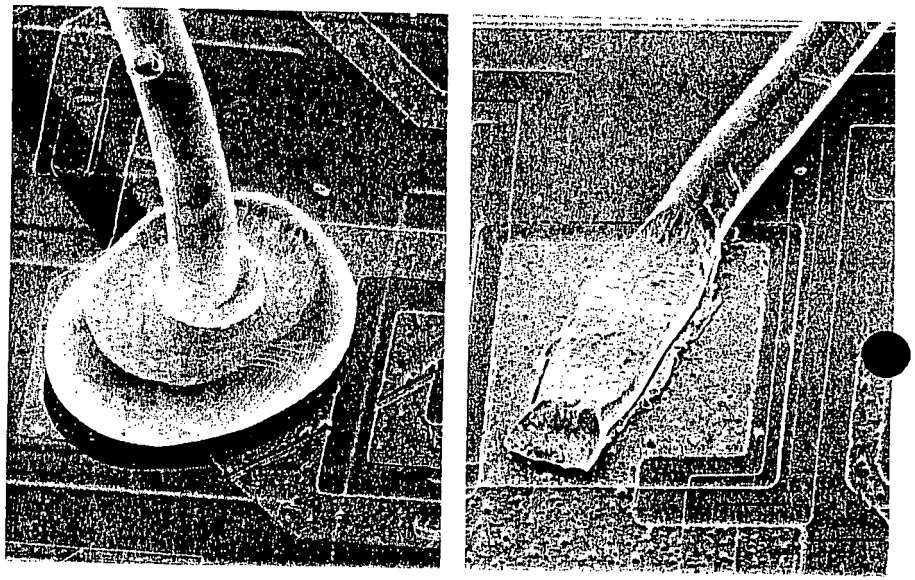

Figure 9-36. Scanning electron micrographs of a ball bond (a) and a wedge bond (b). (Photographs courtesy of the National Bureau of Standards.)

chip is turned upside down, and the bumps are properly aligned with the metallization pattern on the substrate. At this point, ultrasonic bonding or solder alloying attaches each bump to its corresponding connector on the substrate. An obvious advantage of this method is that all connections are made simultaneously. Disadvantages include the fact that the bonds are made under the chip and therefore cannot be inspected visually. Furthermore, it is necessary to heat and/or exert pressure on the chip.

In beam-lead technology, bonds to the substrate pattern are made external to the Si chip. The process is more complicated than flip-chip methods, but there are important compensations. Basically, the beam-lead technique calls for thick (about 10 μm) metal tabs on the wafer, leading away from the circuit at each contact pad. These relatively large ("beam") leads are commonly made by electroplating Au onto the wafer in regions defined by a photoresist pattern. The beam leads extend from the metallized interconnection pattern to outside the active area of each circuit. Then the wafer is mounted face down in wax on a flat disk and is lapped from the back side to a total wafer thickness of about 50 μm. A photoresist pattern is used

SOLID STATE ELECTRONIC DEVICES

second edition

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DECLARATION

I, Samuel Borodach, hereby declare:

1. I am an attorney of record in the application identified above.

2. A true and correct copy of the title page and pages 368-371 of B. Streetman, *Solid State Electronic Devices*, (Prentice-Hall 1980, 2nd ed.) is attached as Exhibit 1.

Respectfully submitted,

Date: 7/17/06

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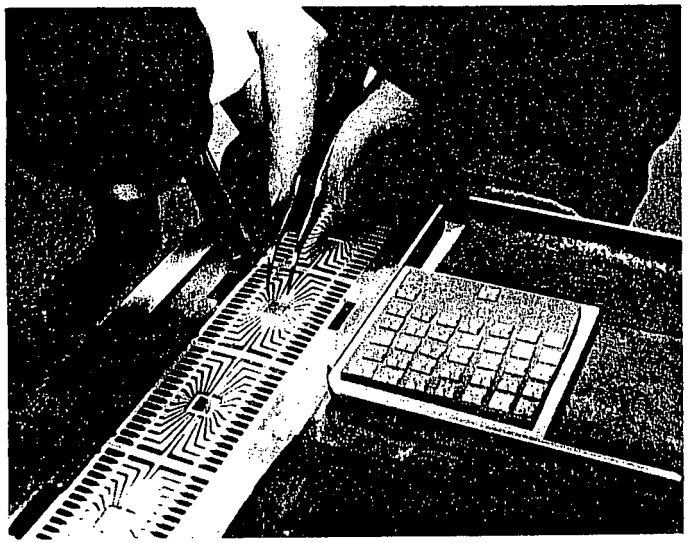

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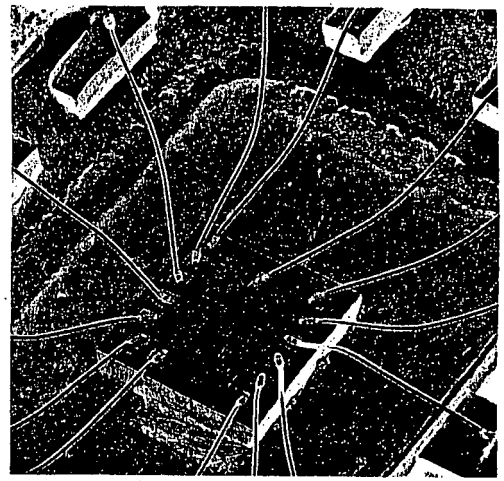

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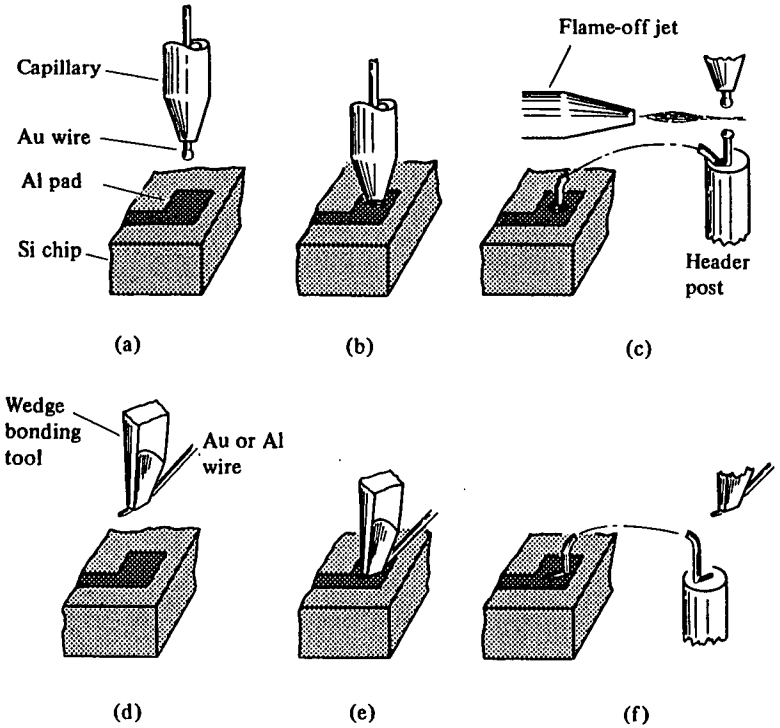

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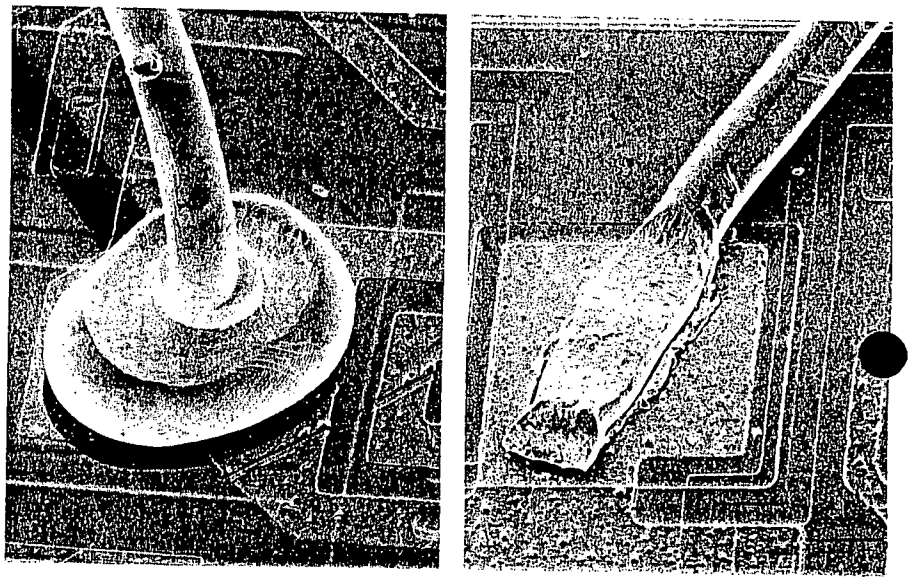

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	: Arnd Kilian et al.	Art Unit	: 2832
Serial No.	: 10/699,981	Examiner	: Tuyen Nguyen
Filed	: November 3, 2003	Conf. No.	: 5328
Title	: THREE-DIMENSIONAL INDUCTIVE MICRO COMPONENTS		

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL LETTER

Correspondence relating to this application is enclosed, including a Brief on Appeal and a Declaration.

The required fee of $250.00 is enclosed. Please apply any charges not covered, or any credits, to Deposit Account No. 06-1050.

Respectfully submitted,

Date: 7/17/06

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